Reg.No. _____

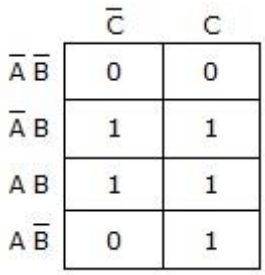
Karunya UNIVERSITY
(Karunya Institute of Technology & Sciences)
(Declared as Deemed-to-be University under Sec.3 of the UGC Act, 1956)

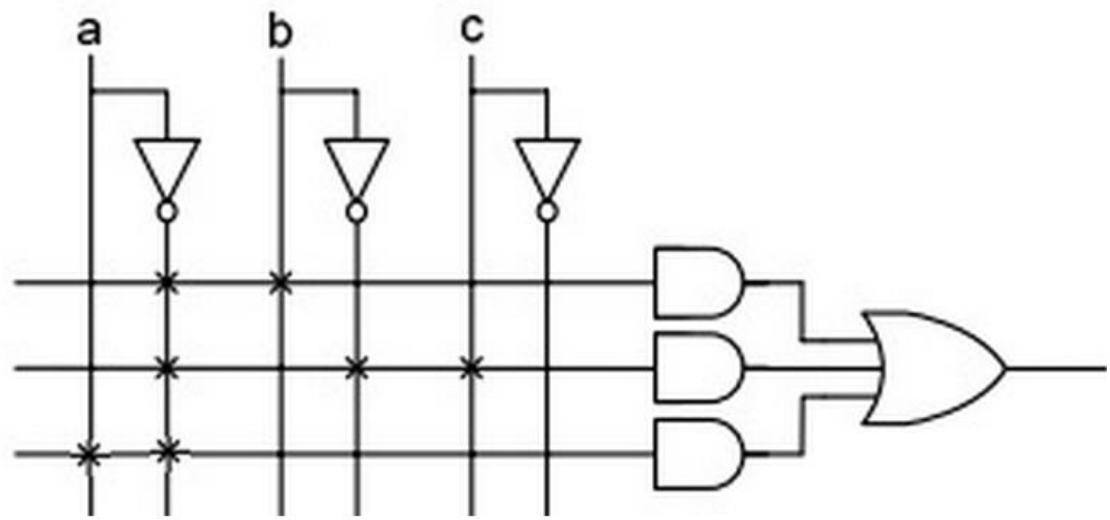
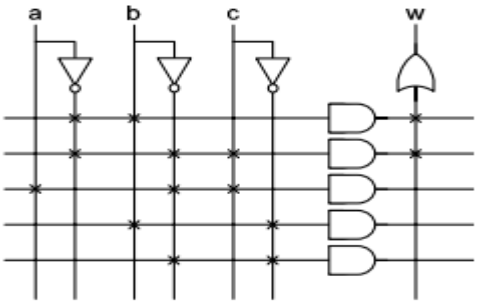
End Semester Examination – Nov/Dec – 2016

Code : 14EC2001 **Semester : 2016-17 ODD**
Sub. Name : Digital Electronics **Duration : 3hrs**
Max. marks : 100

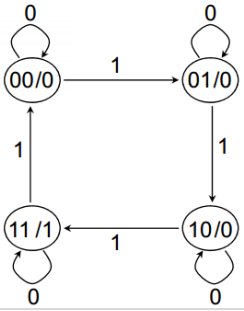
Q. No.	Questions				Course outcome	Marks
	PART-A (40X1=40 MULTIPLE CHOICE QUESTIONS)					
1.	Base 16 refers to which number system?					
	a. binary coded decimal	b. decimal	c. octal	d. hexadecimal		
2.	Convert the binary number $(1011011)_2$ to octal.					
	a. 134	b. 132	c. 133	d. 131	CO1	(1)
3.	Mention the number of independent digits in decimal number system.					
	a. 16	b. 8	c. 10	d. 9	CO1	(1)
4.	What is the 10's complement of $(2496)_{10}$?					
	a. 7503	b. 7502	c. 7505	d. 7504	CO1	(1)
5.	Mention the code in which the consecutive numbers will have single bit change.					
	a. Excess 3 code	b. Gray code	c. Binary code	d. Alphanumeric code	CO1	(1)
6.	Which of the following is the most widely used alphanumeric code for computer input and output?					
	a. ASCII	b.parity	c.BCD	d.hexadecimal	CO1	(1)
7.	Using Boolean algebra write an equivalent expression for XYZ+XY'Z					
	a. X	b.XZ	c.1	d.0	CO1	(1)
8.	From the truth table below, determine the standard SOP expression					
	a. X= (A'.B.C')+(A.B.C) +(A'.B'.C')	b. X= (A'.B'.C)+(A'.B.C) +(A.B.C')	c. X= (A.B.C)'	d. X=A+B+C	CO2	(1)
9.	A + 0 = _____					
	a. 1	b.2A	c.A	d.0	CO1	(1)

Inputs			Output
A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

10.	The simplest equation which implements the K-map shown below is  					
	a. A+BC	b. AB+BC+CA	c. AC+B	d. BC+B	CO2	(1)
11.	An equivalent representation for the Boolean expression A' + 1 is					
	a. 0	b. A	c. 1	d. A'	CO1	(1)
12.	Equivalent representation of NAND gate is					
	a. AND invert	b. invert OR	c. invert AND	d. buffer invert	CO1	(1)
13.	In a Full Subtractor circuit, mention the Difference and Borrow when the inputs are 0,1,1.					
	a. Difference =1 Borrow = 0	b. Difference =1 Borrow = 1	c. Difference =0 Borrow = 1	d. Difference =0 Borrow = 0	CO2	(1)
14.	A logic circuit which receives information from 2^n input lines and transmits this information on a single output line is					
	a. Encoder	b.Decoder	c.Multiplexer	d.Demultiplexer	CO2	(1)
15.	The basic building block of a combinational logic circuit is					
	a. memory	b. flip flop	c. latches	d. Logic Gates	CO2	(1)
16.	BCD to excess code converter input is 0001, output= ----------					
	a. 0010	b.0110	c.0111	d.1000	CO2	(1)
17.	For a 2 bit magnitude comparator A="10" and B="01", outputs (A=B) = ----------, (A<B) = ---------- and (A>B) = ----------					
	a. 1,0,0	b.0,1,0	c.0,0,1	d.1,1,0	CO2	(1)
18.	In positive logic, the logic one state corresponds to					
	a. high voltage level	b. low voltage level	c.medium voltage level	d.negative voltage level	CO2	(1)
19.	A combinational circuit that converts binary information from from 2^n input lines to n output lines is					
	a. encoder	b.multiplexer	c. demultiplexer	d.decoder	CO2	(1)
20.	Mention the expression for carry propagate in a binary parallel adder when the inputs are Ai, Bi, Ci					
	a. Ai AND Bi	b. Ai OR Bi	c. Ai XOR Bi	d. Ai NOR Bi	CO2	(1)
21.	Edge triggered single bit storage device is called as					
	a. flip flop	b. latch	c. register	d. RAM	CO2	(1)
22.	D flip flop is a single input version of					
	a. JK flip flop	b.SR flip flop	c. delay flip flop	d. set flip flop	CO2	(1)
23.	Mention the input condition for RS flipflop to be in set mode.					
	a. R=1,S=1	b.R=1,S=0	c.R=0,S=0	d.R=0,S=1	CO2	(1)
24.	Mention the table that lists the inputs of a flip flop for a known condition of its states					
	a. Truth table	b. State table	c. Excitation table	d. Clock table	CO2	(1)
25.	The terminal count of a modulus-10 binary counter is _____.					
	a. 1001	b. 1011	c. 1100	d. 1010	CO2	(1)
26.	What is the condition for JK flip flop to toggle?					
	a. J=0 and K=0	b. J=1 and K=0	c. J=0 and K=1	d. J=1 and K=1	CO2	(1)
27.	The JK flipflop is in its reset mode when input J = _____ and input K = _____.					
	a. 1 and 1	b.0 and 1	c.1 and 0	d.0 and 0	CO2	(1)

28.	What is the input condition for RS flipflop to remain in an same state?					
	a. R=0,S=0	b.R=1,S=0	c.R=1,S=1	d.R=0,S=1	CO2	(1)
29.	A 4bit up/down binary counter is in the UP mode and in the 1001 state. To what state does the counter go on the next clock pulse?					
	a. 1010	b.1011	c.0111	d.1110	CO2	(1)
30.	A counter counts the _____					
	a. number of clock pulses	b.number of flipflops	c.number of outputs	d.number of inputs	CO2	(1)
31.	How many flip-flops are required to make a MOD-16 binary counter?					
	a. 5	b. 6	c. 16	d. 4	CO2	(1)
32.	How many clock pulses are required to get the output of a 4 bit SISO shift register?					
	a. 4	b. 5	c. 1	d. 8	CO2	(1)
33.	Write equation for the following PAL Implementation. 					
	a. w=(ab)'+abc'+a'	b. W=(a+b)(a'+b'+c)(a)	c. w=ab+abc+a	d. w=a'b+a'b'c	CO3	(1)
34.	Write the expression for the following PLA structure 					
	a. w=(a+b)(a'+b'+c)	b. w=ab+abc	c. w=a'b+a'b'c	d. w=(ab)'+abc'	CO3	(1)
35.	Which of the following is the non saturated logic?					
	a. TTL	b.CMOS	c. Schottky TTL	d.ECL	CO3	(1)
36.	---------- is the amount of noise that a circuit could withstand without compromising the operation of circuit.					
	a. Noise margin	b. Fan out	c. power dissipation	d. propagation delay	CO3	(1)
37.	In ---------- PLD structure both arrays are programmable.					
	a. PROM	b. PLA	c. PAL	d. EPROM	CO3	(1)

38.	The time required for the gate or inverter to change its state is called----------					
	a. Noise margin	b. Fan out	c. power dissipation	d. propagation delay	CO3	(1)
39.	The number of standard loads that the output of the gate can drive without impairment of its normal operation is called----------					
	a. Noise margin	b. Fan out	c. power dissipation	d. propagation delay	CO3	(1)
40.	In PROM ----------arrayfixed and ---------- array programmable.					
	a. AND and OR	b.both AND and OR programmable	c.OR and AND	d.both AND and OR fixed	CO3	(1)

	PART B(8 X 5 = 40 MARKS) (ANSWER ANY EIGHT)		
41.	Draw circuit diagram and write truth table for the following expression Q=AB+AC'	CO1	(5)
42.	Simplify the following using Kmap f(a,b,c)=m(1,2,4)+d(0,3)	CO1	(5)
43.	Draw 4 bit parallel adder diagram.	CO2	(5)
44.	Derive excitation table for JK flip flop	CO2	(5)
45.	Design one bit comparator	CO2	(5)
46.	Implement the following expression using NAND gate AB+C	CO1	(5)
47.	Design 2X4 decoder.	CO2	(5)
48.	Draw Johnson counter diagram and write the sequence table	CO2	(5)
49.	Design MOD-3 counter using T flip flop	CO2	(5)
50.	Implement the following function using PROM f(A,B,C,D)=Σm(0,1,3,5,7,9,12,14)	CO3	(5)
	PART C(2 X 10 = 20 MARKS) (ANSWER ANY TWO)		
51.	Covert the following in to canonical form and write truth table i. Y=ABC+ACD'+A'B ii. Q=AB+AC'D	CO1	(10)
52.	Draw and Explain NAND,NOT and NOR gate CMOS representation.	CO3	(10)
53.	Implement the following circuit using T flip flop 	CO2	(10)

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